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YAN.036

AMENDMENTS TO THE CLAIMS:

1-10. (Canceled)

11. (Currently amended) A charge pump-type booster circuit, comprising:

a pair of input terminals for providing an input voltage, one of said input terminals being connected to a reference voltage level;

a charge capacitor;

a first pair of switches capable of alternatively assuming a first condition, coupling said charge capacitor across said pair of input terminals to charge said charge capacitor to a voltage level substantially equal to the voltage level of the input voltage, and a second condition decoupling said charge capacitor from across said input terminals;

a first output capacitor;

a second pair of switches capable of assuming a first condition, coupling said first output capacitor across a first serial combination, comprising said input terminals and said charge capacitor, to charge said first output capacitor to a voltage level substantially twice the voltage level of the input voltage, and a second condition, decoupling said first output capacitor from said first serial combination;

a second output capacitor; and

a third pair of switches capable of assuming a first condition, coupling said second output capacitor across a second serial combination, comprising said charge capacitor and said first output capacitor, to charge said second output capacitor to a voltage level

substantially three times the voltage level of the input voltage, and a second condition, decoupling said second output capacitor from said second serial combination,

wherein one side of each of said first output capacitor and said second output capacitor is always connected to the reference voltage level.

12. (Previously presented) The charge pump-type booster circuit as set forth in claim 11, further comprising a load connected in parallel with said first output capacitor.

13. (Previously presented) The charge pump-type booster circuit as set forth in claim 11, further comprising a load connected in parallel with said second output capacitor.

14. (Currently amended) A ~~The~~ charge pump-type booster circuit, ~~as set forth in claim 11, further~~ comprising:

a pair of input terminals for providing an input voltage;

a charge capacitor;

a first pair of switches capable of alternatively assuming a first condition, coupling said charge capacitor across said pair of input terminals to charge said charge capacitor to a voltage level substantially equal to the voltage level of the input voltage, and a second condition decoupling said charge capacitor from across said input terminals;

a first output capacitor;

a second pair of switches capable of assuming a first condition, coupling said first output capacitor across a first serial combination, comprising said input terminals and said

charge capacitor, to charge said first output capacitor to a voltage level substantially twice the voltage level of the input voltage, and a second condition, decoupling said first output capacitor from said first serial combination;

a second output capacitor;

a third pair of switches capable of assuming a first condition, coupling said second output capacitor across a second serial combination, comprising said charge capacitor and said first output capacitor, to charge said second output capacitor to a voltage level substantially three times the voltage level of the input voltage, and a second condition, decoupling said second output capacitor from said second serial combination;

a first load connected in parallel with said first output ~~capacitor, and~~ capacitor; and

a second load connected in parallel with said second output capacitor.

15. (Previously presented) The charge pump-type booster circuit as set forth in claim 11, wherein each of said switches comprises a thin film transistor.

16. (Previously presented) A charge pump-type booster circuit, comprising:

a pair of input terminals for providing an input voltage;

a charge capacitor;

a pair of charge switches;

N output capacitors, identified in sequence as output capacitor number 1 to output capacitor number N; and

N pairs of boosting switches, wherein:

said pair of charge switches is capable of alternatively assuming a first condition, coupling said charge capacitor across said pair of input terminals to charge said charge capacitor to a voltage level substantially equal to the voltage level of the input voltage, and a second condition decoupling said charge capacitor from across said input terminals,

a first one of said pairs of boosting switches is capable of alternatively assuming a first condition, coupling output capacitor number 1 across a first serial combination, comprising said input terminals and said charge capacitor, to charge output capacitor number 1 to a voltage level substantially twice the level of the input voltage, and a second condition decoupling output capacitor number 1 from said first serial combination,

a second one of said pairs of boosting switches is capable of alternatively assuming a first condition, coupling output capacitor number 2 across a second serial combination, comprising said charge capacitor and output capacitor number 1, to charge output capacitor number 2 to a voltage level substantially three times the input voltage level, and a second condition decoupling output capacitor number 2 from said second serial combination,

each of the remaining pairs of boosting switches is capable of assuming a first condition, coupling an associated output capacitor number n across an associated serial combination, comprising output capacitor number (n-2) and output capacitor number (n-1), to charge said output capacitor number n to a voltage level at least equal to (n+1) times the input voltage level,

N is an integer greater than 2, and

n is an integer greater than 2 and less than or equal to N.

17. (Previously presented) The charge pump-type booster circuit as set forth in claim 16, further comprising a load connected in parallel with one of said output capacitors.

18. (Previously presented) The charge pump-type booster circuit as set forth in claim 16, further comprising a plurality of loads, each load connected in parallel with one of said output capacitors.

19. (Previously presented) The charge pump-type booster circuit as set forth in claim 16, further comprising n loads, each load connected in parallel with one of said output capacitors.

20. (Previously presented) The charge pump-type booster circuit as set forth in claim 16, wherein each of said charge switches and each of said boosting switches comprise a thin film transistor.